



## Digital Satellite Equipment Control (DiSEqC™)



# RESET CIRCUITS FOR THE SLAVE MICROCONTROLLER

August 12, 1996

**Reference Documents that define the DiSEqC System:**

DiSEqC™ Bus Specification Version 4.2 (February 25, 1998)

DiSEqC™ Slave Microcontroller Specification Version 1.0 (February 25, 1998)

DiSEqC™ Logos and Their Conditions of Use (February 25, 1998)

**Associated Documents:**

Update and Recommendations for Implementation Version 2.1 (February 25, 1998)

Application Information for using a "PIC" Microcontroller in DiSEqC™ LNB and simple switcher Applications Version 1.0 (June 7, 1999)

Application Information for Tuner-Receiver/IRDs (April 12, 1996)

Application Information for LNBs and Switchers Version 2 (February 25, 1998)

Reset Circuits for the Slave Microcontroller (August 12, 1996)

Simple Tone Burst Detection Circuit (August 12, 1996)

Positioner Application Note Version 1.0 (March 15, 1998)

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# 1. Introduction

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The DiSEqC Slave Microcontroller is a custom-programmed version of the Philips Semiconductors 8xC750 general purpose microcontroller. As such, it requires a simple external reset circuit connected to the Reset pin. This is to ensure that the microcontroller starts from a defined state and does not attempt to perform any control functions until the power supply is fully established and the timing oscillator is operating with a stable (full) amplitude.

In many microcontroller applications, the initialisation time is not critical so a relatively long reset time can be employed. However, most DiSEqC accessories are expected to be powered via the bus, and some "distant" ones (i.e. not connected directly to the cable from the Tuner-Receiver/IRD) may receive power only when another device switches them in, for example when the user selects a new channel to view. In this case a rapid response is required, so attention must be paid to the hardware reset time.

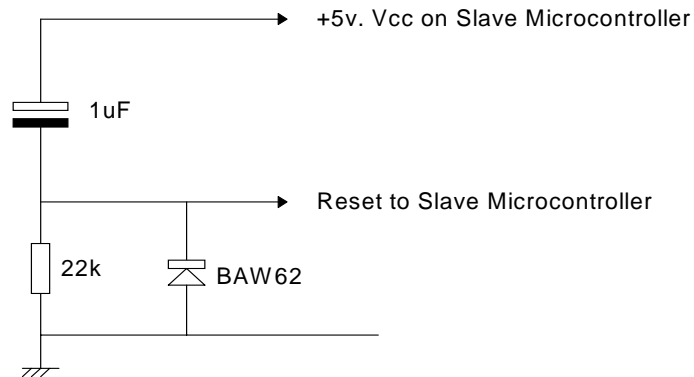
# 2. Simple Reset circuit for DiSEqC-Compliant Tuner-Receiver/IRDs

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It is recommended that all DiSEqC Tuner-Receiver/IRDs should apply power to the bus quite rapidly (with a rise-time of typically 5 ms) so that a simple edge-triggered reset circuit (with a reset delay of typically 20 - 50 ms) may be used in all Slaves.

The simplest way to achieve a reset time of approximately 20 ms with the 8xC750 microcontroller is to use just a reset capacitor of typically 220 nF from the Reset pin to the Vcc supply rail. However, the reset time is then dependent on the sink current defined by the microcontroller, which has very wide tolerances. Therefore, the preferred arrangement is to use a reset capacitor of typically 1  $\mu$ F and an additional resistor of typically 22 k $\Omega$  to ground, as shown in Figure 1.

The optional diode rapidly discharges the capacitor when the supply voltage falls, to ensure that a reset occurs if the supply voltage is interrupted only briefly.



**Figure 1: Simple Time-delay Reset circuit**

### 3. Voltage-dependent Reset circuit

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Some Tuner-Receiver/IRDs (not compatible with the DiSEqC Specification) may give a slowly-rising d.c. voltage on the I.F. download cable when they are switched on (perhaps because they employ a “slow-start” mains power supply). This may cause an unsatisfactory start-up of some accessories including Slaves which employ the short time-constant reset described above. One solution is to use a commercial 3-terminal “Reset Supervisory I.C.” in each Slave application, to ensure that the reset pin is only released when the d.c. supply voltage is fully established. An “active-high reset” type is required, and also such a device may be considered unduly expensive. Therefore, Figure 2 shows a simple voltage-dependent reset circuit which makes use of the 3-terminal voltage regulator already included for the microcontroller.

The method of operation is that when the supply voltage initially rises, the series element in the 3-terminal regulator is saturated, with typically a 1 volt drop from input to output. The transistor is therefore brought into conduction by the resistor from its base to ground, and generates the positive reset signal. Only when the supply rail is fully established (with typically 3 volts or more between the regulator’s input and output terminals) is the voltage at the transistor’s base pulled high enough to switch off the transistor and release the reset pin. A capacitor delay is included in case the supply rises very rapidly but the (crystal) oscillator starts slowly. A diode is not needed because the transistor discharges the capacitor as soon as the input voltage starts to fall below the threshold.

Note that the reverse base-emitter breakdown voltage (usually >6 volts) must not be exceeded so if input voltages of typically greater than 20 volts may be encountered then a protection diode should be used either across the (reverse) base-emitter junction, or in series with the base. Small-value electrolytic capacitors are shown to indicate their polarity, but unpolarised types are equally suitable.

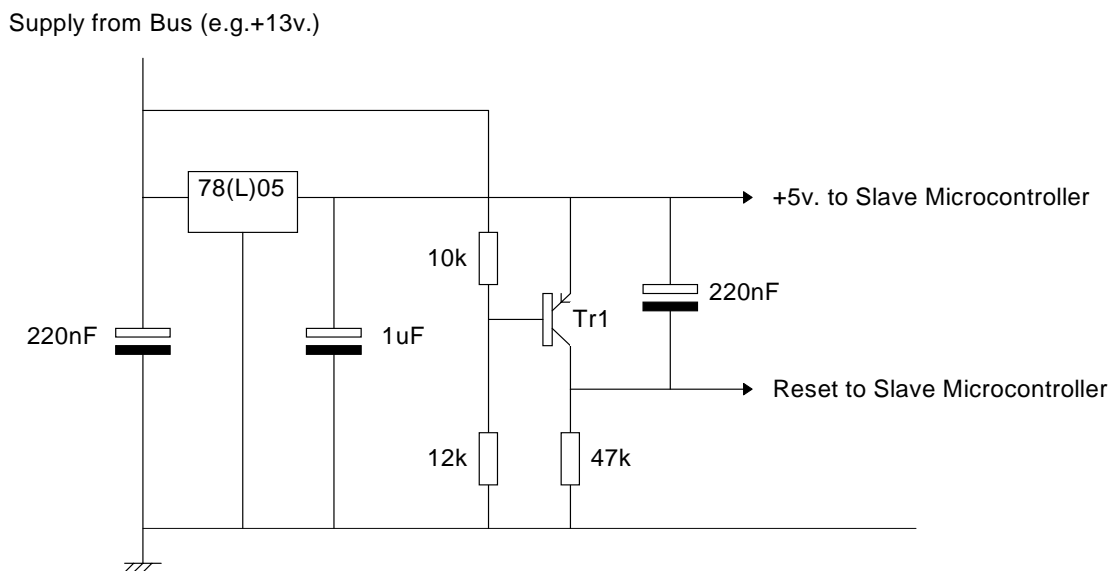


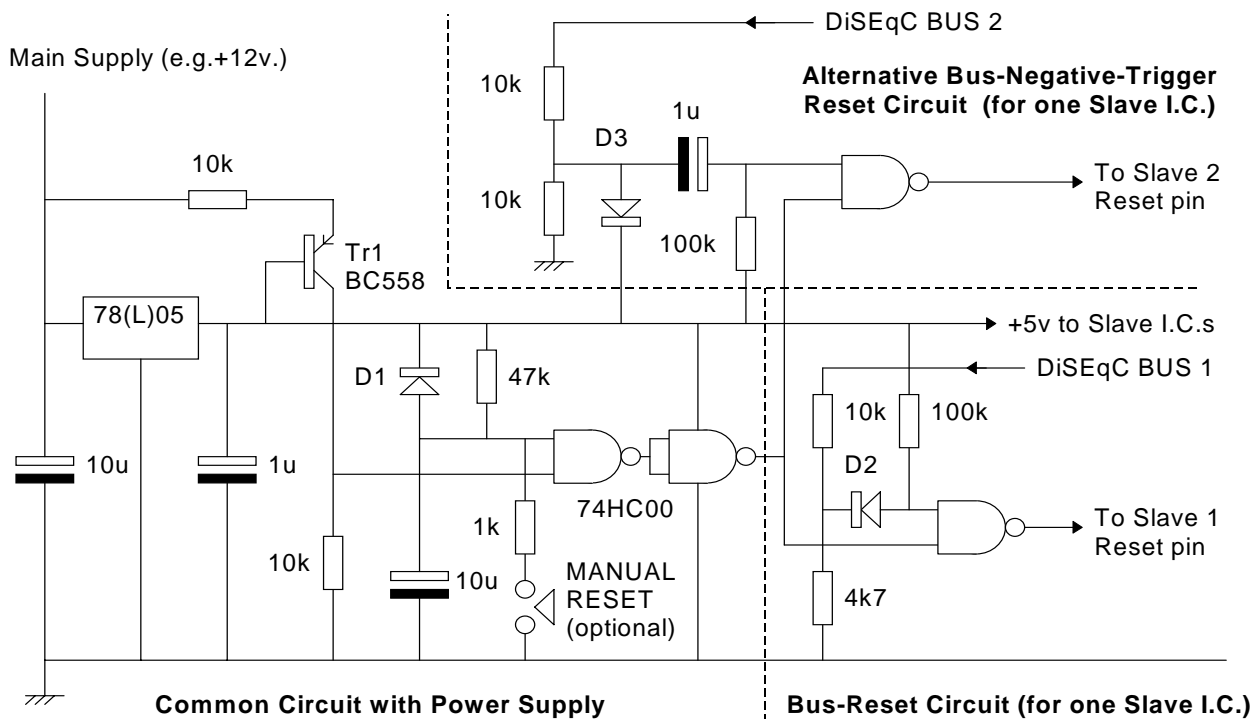
Figure 2: Voltage-threshold reset circuit

## 4. Reset Circuit for SMATV Applications

In SMATV applications it is more usual for a number of Slave switches to be grouped together and to be powered from a common, local supply rather than along each output cable (bus). The reset circuit requirements are thus rather different to those for LNBS or simple Switchers.

The simplest form could use a single, large-value capacitor (giving a reset delay longer than the rise-time of the local power supply) feeding the Reset pins of all the Slave microcontrollers. However, in all microprocessor-based systems it is wise to give the user (viewer) the ability to cause a hardware-reset, in case software problems arise, for example because of electrical disturbance. The method used here is to make the reset of each Slave microcontroller dependent on the d.c. voltage fed along its associated cable.

Figure 3 includes two possible configurations, one generating a reset whenever there is no d.c. voltage on the bus, and the other only for a short time when the d.c. voltage falls to zero. The overall design is most economical when there are a number of Slave I.C.s operating from a single power supply, because it consists of two parts; a common part with the power supply, and only a simple reset gate section which is duplicated for each Slave I.C.



**Figure 3: Externally-Powered SMATV reset circuit**

The principle of operation is that the Slave I.C. is powered only from the local (external) power supply, and the Reset pin (for each I.C.) is released (i.e. 0 volts, allowing the Slave to run) only when 3 conditions are valid:

- The power supply is stabilised at 5 volts
- There has been a start-up time delay
- There is a d.c. voltage on the bus.

With this arrangement the DiSEqC Slave cannot reply to the Master if there is no local power (but it does not put an excessive load on the bus and prevent other accessories from communicating). This is simpler than trying to make the I.C. switch to take power from the bus when the local power is not available.

Similarly, the Slave does not respond when there is no d.c. voltage on the bus (because the reset is forced), but this is the same situation as if the I.C. were powered from the bus. However, the diagram also shows an alternative edge-triggered configuration, for situations where it is necessary for the Slave to operate when there is no d.c. voltage on the bus.

The gates should be HCMOS types so that their nominal input switching level is  $\frac{1}{2}$  of the Vcc supply voltage. There are four NAND gates in a device such as 74HC00, so one package can feed 2 Slave I.C.s, and two packages can feed 6, etc. An alternative could be the 74HC132 which has some “Schmitt trigger” hysteresis to give more stable outputs if any of the signals are “dirty”.

Tr1 and the two 10k resistors are a simple detector that the 78(L)05 is in regulation. Only when there is more than about 3 volts across the series regulator (i.e. 8 volts input) is there enough current in the lower resistor to pull the gate input “high”. As an alternative, a commercial 3-terminal “reset supervisory I.C.” could be used on the 5 volt rail, such as Zetex ZM33064 or Telcom VC4302EZH, but these seem rather more expensive. Note that they produce an “active low” (reset) which would be inverted by the gate.

D1 ensures that the start-up delay capacitor is discharged even if the supply voltage falls to 0 volts for only a short time, and the optional push-button can reset all the Slaves in applications where it is inconvenient to disconnect the external power supply.

In the d.c. reset version, D2 and the 100k resistor are not essential (because the on-chip input protection diodes will restrain the input voltage), but D2 prevents the bus voltage being fed into the +5 volt Vcc rail, which might cause problems in some applications.

The alternative edge-triggered Capacitor/Resistor coupling could be used so that the reset occurs when the bus voltage falls to OFF. (Probably a slightly different arrangement could be devised if it was necessary to generate the reset when the d.c. voltage is switched ON). This edge detector network only starts to operate when the voltage falls below about 10 volts, so that the reset does not occur with 13/17 volt level changes.

Note that in this edge-triggered reset circuit, D3 and the 100k resistor are connected to the +5 volt Vcc rail, and that current sometimes flows in the on-chip input protection diodes of the MOS gate. In the stable state there is a slight reverse voltage (one forward diode drop, approximately 0.6 volt) across the electrolytic capacitor, but this is generally considered acceptable.